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| International Application Number: | |
| Confirmation Number: | 4982 |
| Title of Invention: | INTEGRATED CIRCUIT LOGIC WITH SELF COMPENSATING BLOCK DELAYS |
| First Named Inventor/Applicant Name: | Puneet Gupta |
| Customer Number: | 33233 |
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| 1 | Information Disclosure Statement (IDS) Filed | US_IDS_Form__SB_08a.pdf | 779966 | no | 4 |
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| 2 | NPL Documents | YOR920040091-1.pdf | 477200 | no | 8 |
| | | | ad561d6d36e9b0b85144b77b7c3e36dd 24ee3b29 | | |

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| 3 | NPL Documents | YOR920040091-2.pdf | 873807 | no | 14 |
| | | | e9a00cd45f1c159a100258b76eb7a8f3 909644ad | | |

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| 4 | NPL Documents | YOR920040091-3.pdf | 810731 | no | 13 |
| | | | 56eb655cd3a845eb172a2c9a61f535c2 35b5671 | | |

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| 5 | NPL Documents | YOR920040091-4.pdf | 193308 | no | 9 |
| | | | 03261a87238e4b9741a2d024872865 e59eb062 | | |

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